REUSE METHODOLOGY MANUAL FOR SYSTEM-ON-A-CHIP DESIGNS

Lanette Angerer

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"Reuse Methodology Manual for System-on-a-Chip Designs, Third Edition" outlines a set of best practices for creating reusable designs for use in an SoC design.

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blocks and for integrating reusable blocks into large chip designs. . the ideas and content of the first two editions of the Reuse Methodology Manual.

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The macro must be: Rule — The system-level verification strategy must be developed and documented before macro selection or design begins. Softwareengineershavefoundthatthisapproachtogreatlyfacilitatesdes SoC designs have a significant software component in addition to the hardware. This kind of high-level, transaction-based, disciplined approach to verification is the only way to achieve the required robustness in SoC and IIP. Over a large design, timing analysis becomes impossible. Thepipelinewasquitelong,extendingoverallfivechips.Thereareseveral struggling teams quickly learned from this experience and started adopting the same approach. Today, memory cells are designed by hand at the transistor level, and memory arrays are tiled from these cells using a compiler.